CLAIMS

What is claimed is:

1 -15. (Cancelled)

16. (Original) A method for forming a semiconductor device comprising:

providing a substrate having a surface;

forming an insulating layer over the surface of the substrate;

forming a first patterned conductive layer over the insulating layer;

forming a second patterned conductive layer over the first patterned conductive layer;

forming a patterned non-insulating layer over the second patterned conductive layer; and

selectively removing portions of the first and second patterned conductive layers to form a notched control electrode for the semiconductor device.

17. (Original) The method of claim 16, further comprising implanting source/drain regions in the substrate.

18. (Original) The method of claim 16, further comprising forming a halo implant in the substrate.

19. (Original) The method of claim 16, wherein forming the patterned non-insulating layer comprises forming the patterned non-insulating layer of polysilicon.

20. (Original) The method of claim 16, wherein the first patterned conductive layer comprises one of tantalum carbide, tantalum nitride, nickel silicide, tantalum silicide, cobalt silicide, or tungsten.

21. (Original) The method of claim 16, wherein the first patterned conductive layer comprises one of titanium nitride, rhenium, platinum, ruthenium oxide, rhodium silicide, palladium silicide, or tungsten carbon nitride.

22. (Original) The method of claim 16, wherein the first patterned conductive layer is formed to a thickness of between 1 and 40 nanometers.

23. (Original) The method of claim 16, wherein the second patterned conductive layer comprises silicon germanium.

24. (Original) The method of claim 16, wherein the second patterned conductive layer comprises one of doped silicon germanium, doped silicon, doped silicon carbide, silicide, metal carbide or metal nitride.

25. (Original) The method of claim 16, wherein the insulating layer comprises one of hafnium oxide, aluminum nitride, aluminum oxide, tantalum pentoxide, barium titanium oxide, lanthanum aluminate or zirconium oxide, or combinations thereof.

26. (Original) The method of claim 16, wherein selectively removing portions of the first and second patterned conductive layers further comprises:

selectively etching a predetermined portion of an exposed lateral edge of the second patterned conductive layer; and

oxidizing an exposed portion of the first patterned conductive layer.

27. (Original) The method of claim 16, wherein selectively removing portions of the first and second patterned conductive layers further comprises:

selectively etching a predetermined portion of an exposed lateral edge of the second patterned conductive layer; and

selectively etching an exposed portion of the first patterned conductive layer of the using a soft etch semiconductor manufacturing process.

28. (Original) The method of claim 16, further comprising forming a second insulating layer in the notches and on the opposite sides of the notched control electrode.

29. (Original) The method of claim 16, further comprising forming sidewall spacers on the second insulating layer on the opposite sides and in the notches of the notched control electrode.

30. (New) The method of claim 16, wherein after selectively removing portions of the first and second patterned conductive layers, the first and second patterned conductive layers have lengths that are substantially equal.